

Parasitic Effects Induced by Power Strips Current Switching in Full Wafer Package

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Parasitic effects induced by current switching in power lines for full wafer packages (monolithic or hybrid) are analyzed in the time domain. Theoretical results allow to give simple relations in order to easily predict: * the dynamic drop voltage on the power line, * the parasitic voltages on signal lines, induced by coupling with power line. Experimental measurements on typical devices validate these formula.

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